To: Jeanne DiGrazio
From: Bode Fagbohunka
Subject: Online Search
Date:- March 12, 2003

Please find attached the results of your search for 09667763. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka
703-605-1726

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Set     Items   Description
S1        912   AU=(RYU J? OR RYU, J?)
S2    1309544   COATING? ? OR COAT? OR COATED
S3      35779   SURFACE()TENSION?
S4    2265305   SUBSTRATE? OR IC OR WAFER? OR INTEGRATED()CIRCUIT? OR SEMI-
              CONDUCT? OR SEMI()CONDUCT?
S5          1   S1 AND S2 AND S3 AND S4
S6         16   S1 AND S2 AND (S3 OR S4)
S7         15   S6 NOT S5
S8         15   IDPAT (sorted in duplicate/non-duplicate order)
S9         15   IDPAT (primary/non-duplicate records only)
? logoff
       12mar03 12:01:56 User267146 Session D755.2
             $0.64    0.062 DialUnits File344
     $0.64  Estimated cost File344
             $9.53    0.871 DialUnits File347
                $4.40  4 Type(s) in Format  3
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    $13.93  Estimated cost File347
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    $13.04  Estimated cost File348
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                $5.86  2 Type(s) in Format  9
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    $53.31  Estimated cost File350
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                $9.60  6 Type(s) in Format  3
             $9.60  6 Types
    $17.83  Estimated cost File349
            OneSearch, 5 files,  8.515 DialUnits FileOS
     $3.02  TELNET
   $101.77  Estimated cost this search
   $101.77  Estimated total session cost   8.681 DialUnits


Logoff: level 02.12.60 D  12:01:56

You are now logged off
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9/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014966432 **Image available**
WPI Acc No: 2003-026946/200302
XRAM Acc No: C03-006157
Tape ball grid array semiconductor **package has enhanced wire bonding property by improving a surface structure of a plating layer formed to a stiffener or a heat sink**
Patent Assignee: SAMSUNG TECHWIN CO LTD (SMSU)
Inventor: BOK G S; NOH H H; **RYU J C**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002053253	A	20020705	KR 200082752	A	20001227	200302	B

Priority Applications (No Type Date): KR 200082752 A 20001227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002053253	A		1	H01L-023/12	

Abstract (Basic): KR 2002053253 A
NOVELTY - A TBGA (Tape Ball Grid Array) **semiconductor** package has enhanced wire bonding property by improving a surface structure of a plating layer formed to a stiffener or a heat sink.
DETAILED DESCRIPTION - A copper pattern layer (41b) is formed on the tape (41a) and a photo solder resist (41c) is formed on a part not having the copper pattern layer. The chip is wire-bonded by the copper pattern layer, and the first wire (47a) and the first solder ball (49a) connecting to a terminal of an external **substrate** are adhered to an upper part of the copper pattern layer. The plating layer (400) is plated on an upper surface of the stiffener and is electrically connected to the copper pattern layer via a through hole (420). The second solder ball (49b) having a grounding function is adhered to the upper surface of the copper pattern layer. The oxide **coating** layers (43b, 45b) are respectively formed on an outer surface of the stiffener and the heat sink in order to enhance the adhesive strength between the first and the second adhesive (42 ,44). The first adhesive is interposed between the circuit tape and the stiffener and the second adhesive is interposed between the stiffener and the heat sink.
pp; 1 DwgNo 1/10
Title Terms: TAPE; BALL; GRID; ARRAY; **SEMICONDUCTOR** ; PACKAGE; ENHANCE; WIRE; BOND; PROPERTIES; IMPROVE; SURFACE; STRUCTURE; PLATE; LAYER; FORMING; STIFFEN; HEAT; SINK
Derwent Class: L03; U11
International Patent Class (Main): H01L-023/12
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C17; L04-C21
Manual Codes (EPI/S-X): U11-D01A1; U11-D01A3; U11-D01A5; U11-D02B1; U11-E02A1

9/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011189127 **Image available**
WPI Acc No: 1997-167052/199716
XRAM Acc No: C97-054121

XRPX Acc No: N97-137347

Prodn. of multilayered circuit substrate **- by** coating **upper side of** substrate **with light-sensitive insulating layer, irradiating and developing layer, etc.**

Patent Assignee: SAMSUNG AEROSPACE IND LTD (SMSU); SANSEI KOKU SANGYO KK (SANS-N); SAMSUNG AEROSPACE IND CO LTD (SMSU)

Inventor: **RYU J** ; RYOO J C

Number of Countries: 005 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19636735	A1	19970313	DE 1036735	A	19960910	199716	B
JP 9130051	A	19970516	JP 96257799	A	19960906	199730	
TW 304323	A	19970501	TW 96110973	A	19960907	199730	
KR 97019795	A	19970430	KR 9529688	A	19950912	199820	
US 5747222	A	19980505	US 96712117	A	19960911	199825	
KR 155877	B1	19981215	KR 9529688	A	19950912	200034	
US 6074728	A	20000613	US 96712117	A	19960911	200035	N
			US 97991778	A	19971216		

Priority Applications (No Type Date): KR 9529688 A 19950912; US 97991778 A 19971216

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19636735	A1		8	H05K-003/46	
JP 9130051	A		6	H05K-003/46	
TW 304323	A			H05K-003/46	
KR 97019795	A			H05K-003/46	
US 5747222	A			G03C-005/00	
KR 155877	B1			H05K-003/46	
US 6074728	A			B32B-003/00	Div ex application US 96712117 Div ex patent US 5747222

Abstract (Basic): DE 19636735 A

Prodn. of multilayered circuit **substrate** comprises: (a) **coating** the upper side of a **substrate** (10) with a light-sensitive insulating layer (20); (b) irradiating and developing the insulating layer to form an insulating layer with a pattern (20A) and pattern intermediate spaces (22); (c) forming a conducting layer (30) by compressing conducting ink into the intermediate spaces; (d) forming a number of layers by repeating the above steps; (e) **coating** the upper layer of the layers in (d) with an adhesive insulation layer; (f) forming a thin metal layer on the adhesive insulation layer by thermally pressing and etching the thin metal layer to form a thin metal layer pattern; (g) forming a through-hole (70) in which a conducting material is implanted. The **substrate** , conducting layers, light-sensitive insulation layers, and thin metal layer are in electrical connection. The multilayered circuit **substrate** produced is also claimed.

ADVANTAGE - The circuit **substrate** has an improved surface structure.

Dwg.1A/3

Title Terms: PRODUCE; MULTILAYER; CIRCUIT; **SUBSTRATE** ; **COATING** ; UPPER; SIDE; **SUBSTRATE** ; LIGHT; SENSITIVE; INSULATE; LAYER; IRRADIATE; DEVELOP; LAYER

Derwent Class: L03; P73; U11; V04

International Patent Class (Main): B32B-003/00; G03C-005/00; H05K-003/46

International Patent Class (Additional): C09D-011/00; H01L-021/48; H01L-023/12; H05K-001/02; H05K-001/03; H05K-001/09

File Segment: CPI; EPI; EngPI

Manual Codes (CPI/A-N): L03-H04E3

Manual Codes (EPI/S-X): U11-E02; V04-Q05; V04-R05A